

COMPAL CONFIDENTIAL

MODEL NAME : Goliad MLK 12 UMA ENTRY  
PCB NO : LA-A972P  
BOM P/N : 4319RK31LXX  
GPIO MAP: 3.3b

Goliad MLK 12" UMA ENTRY  
Broadwell U Processor

2013-12-23  
REV : 0.2 (X01)

- @ : Nopop Component
- EMC@ : EMI, ESD and RF Component
- @EMC@ : EMI, ESD and RF Nopop Component
- CXDP@ : XDP Component
- CONN@ : Connector Component
- VPRO@ : Vpro Component
- NVPRO@ : Non-Vpro Component

Layout Dell logo




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REV: X01  
PWB: FGFC2  
DATE: 1352-01

MB PCB	
Part Number	Description
DA800018000	PCB 14A LA-A972P REV0 MB W/O DOCKING 2

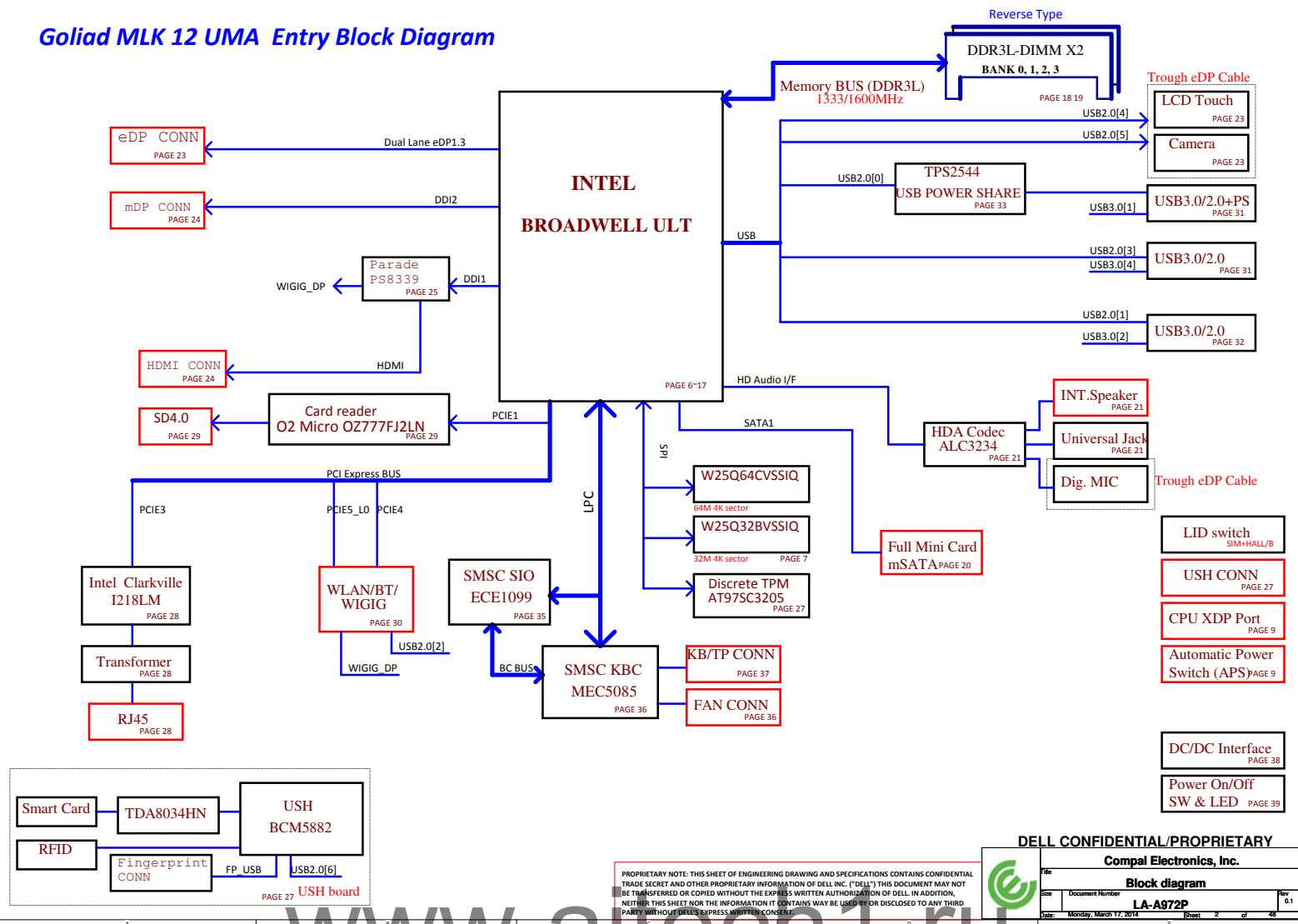
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Goliad MLK 12 UMA Entry Block Diagram



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## POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN - JNGFF1
PCIE 5			WiGig - JNGFF1
PCIE 6		SATA 3	NA
		SATA 2	NA
		SATA 1	JMINI3
		SATA 0	NA

## PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

	USB PORT#	DESTINATION
BDW ULT	0	JUSB1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

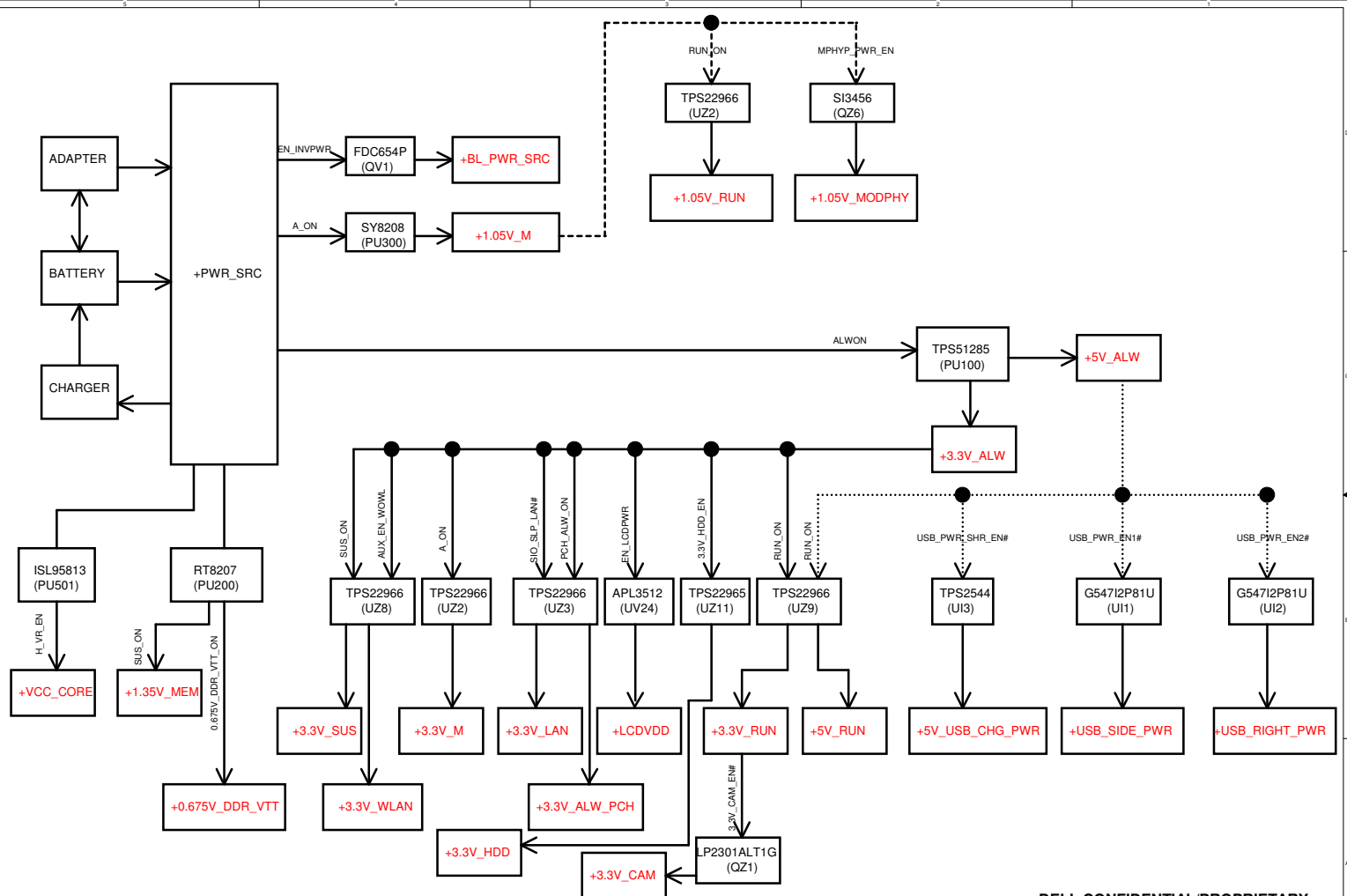
USH	0	BIO
	1	NA

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Power rails

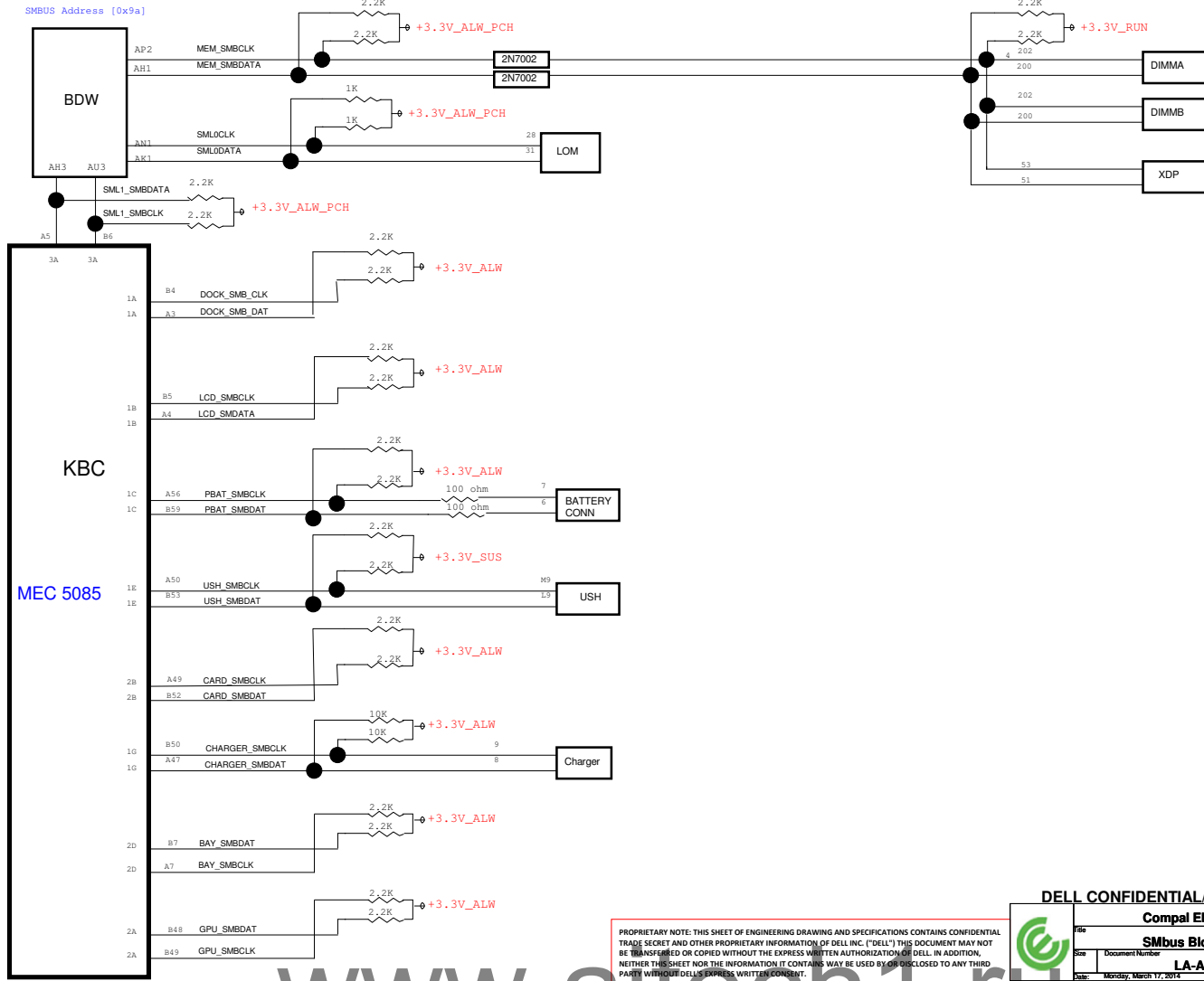
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SMBUS Address [0x9a]



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SMBus Block diagram

LA-A972P

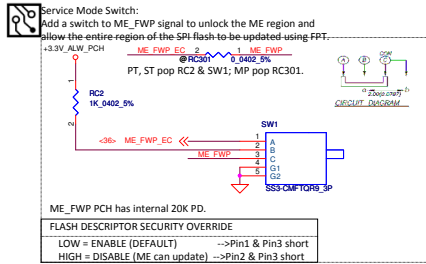
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# UMA SATA port

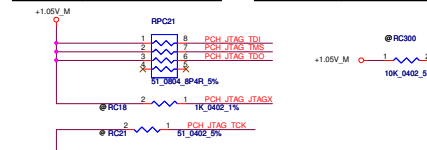
SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0	
E-Dock	mSATA	G12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	mSATA	G12 Entry	NA	NA	
E-Dock	mSATA	G14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	G14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	mSATA	G14D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	G14U_En	NA	NA	



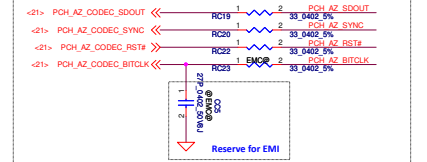
INTVRMEN - INTEGRATED SUS 1.05V VRM  
ENABLE  
High - Enable Internal VRs  
Low - Enable External VRs

ME\_CLR1  
Shunt  
Open  
Keep ME RTC Registers

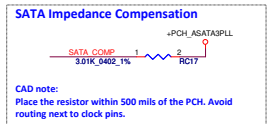
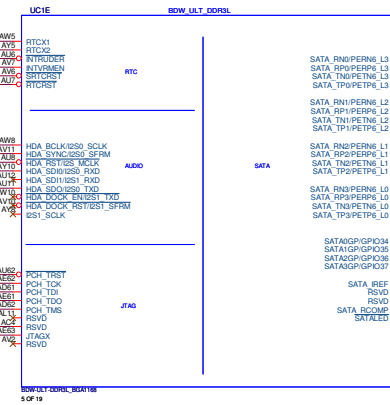
CMOS\_CLR1  
Shunt  
Open  
Clear CMOS



## HDA for Codec



Reserve for EMI

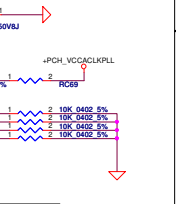
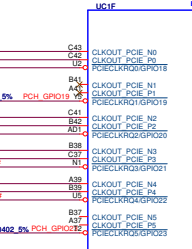
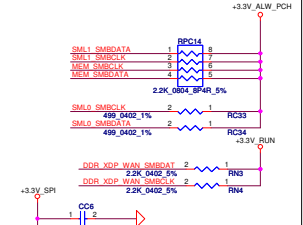


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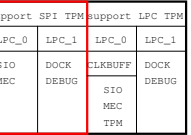
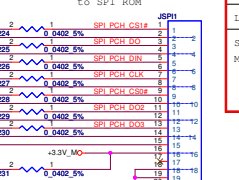
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CPU (1/12)	
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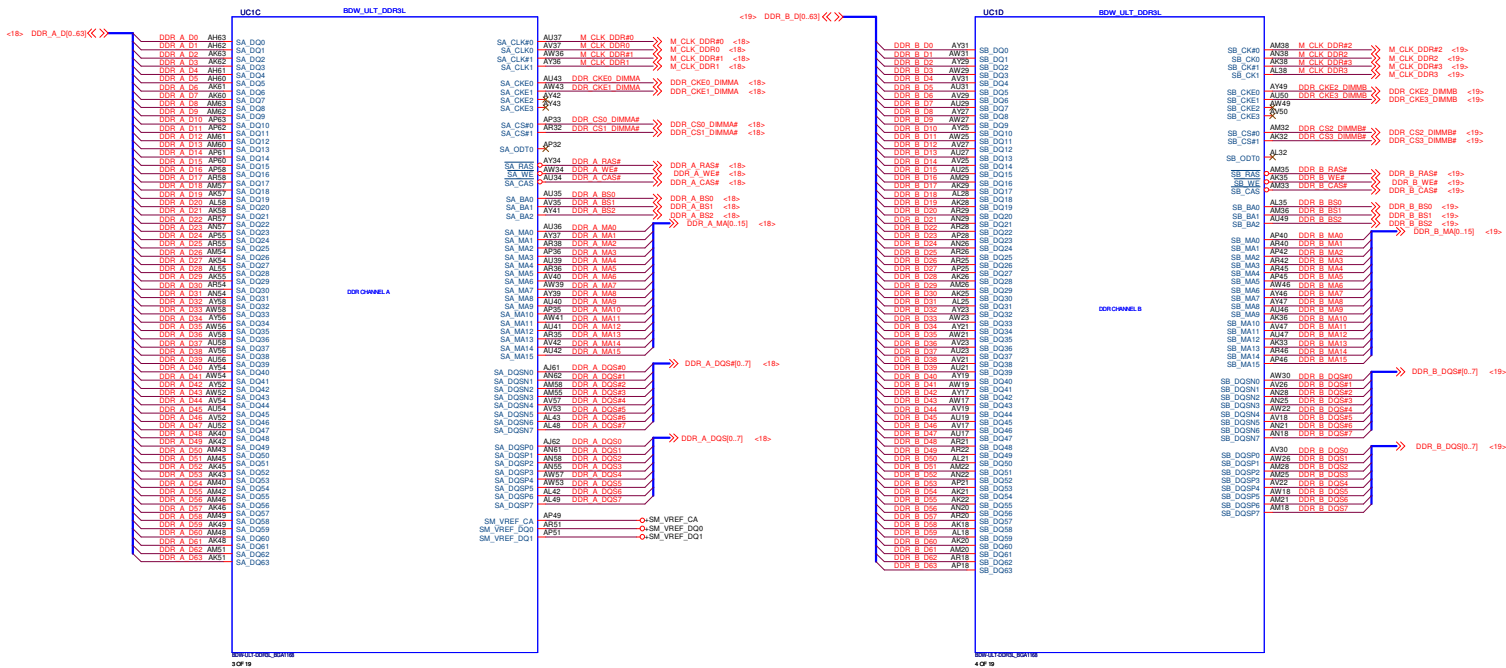
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Timing diagram for EMI reserve showing two signal traces: CLK\_PCLK\_LPC\_0 EMC@ RC74\_1 and CLK\_PCLK\_LPC\_1 EMC@ RC67\_1. Both traces show a transition from high to low, with a delay of 22.040 ns indicated. Below the traces, two signal paths are shown: CLK\_PCLK\_MEG 12P\_0402\_50VBJ and CLK\_PCLK\_LPDEBUJ 12P\_0402\_50VBJ, both connected to EMC@ CC12 and EMC@ CC13 respectively. The diagram is labeled "Reserve for EMI".



Please place RC224~RC331 with JSPI1 at the same MB side



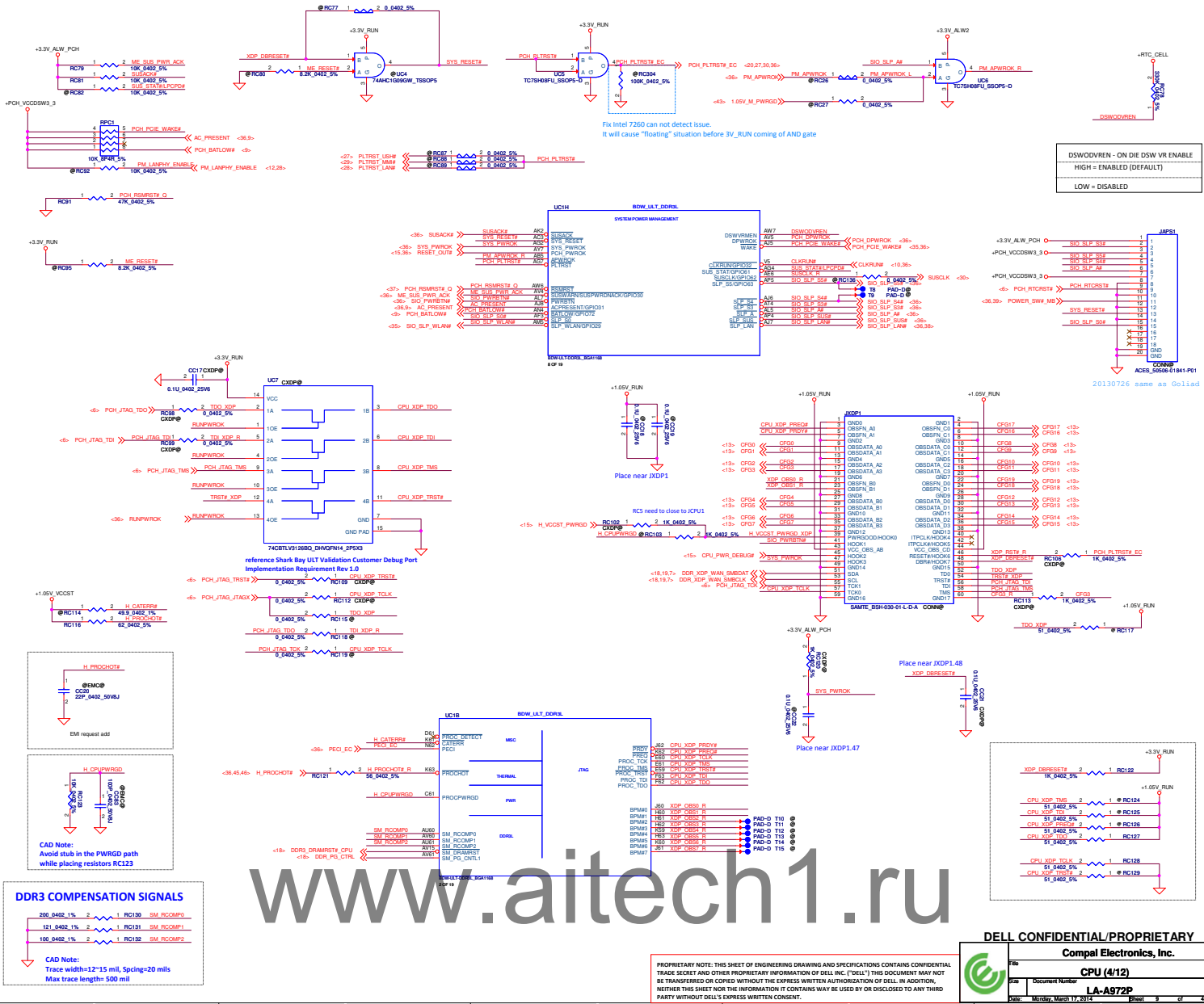
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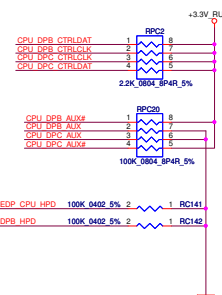
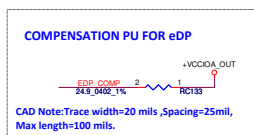
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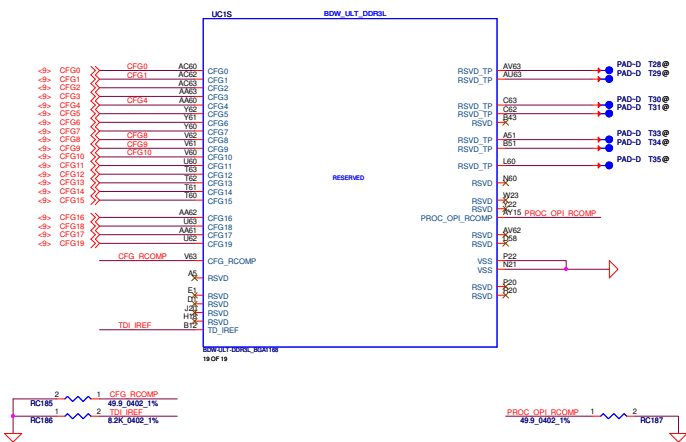
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CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed

SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked 0:Disable Noa will be available pegrardless of the locking of the unit

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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CPU (8/12)

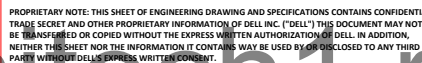
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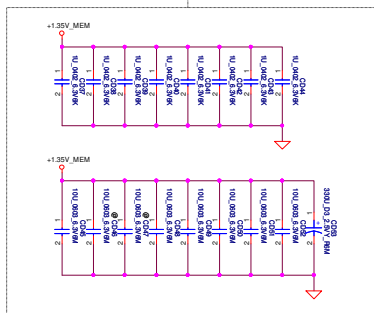




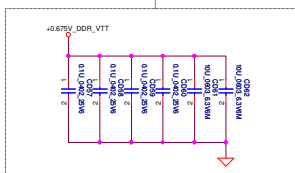
# H=4mm Reverse Type

DDR\_B\_D0[4:7] <<>  
DDR\_B\_D0[4:7] <<>  
DDR\_B\_D0[4:7] <<>  
DDR\_B\_Map[1:1] <<>

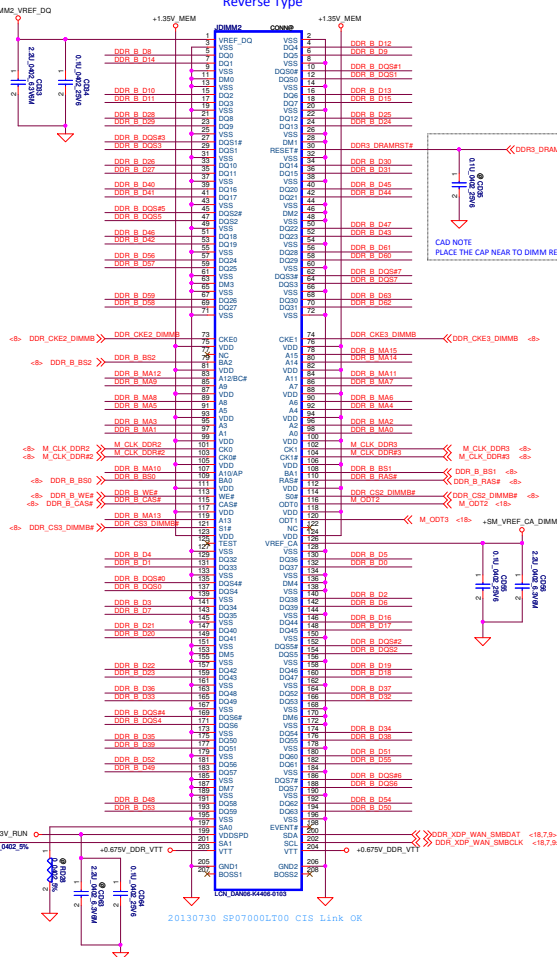
Layout Note:  
Place near JDIMM2



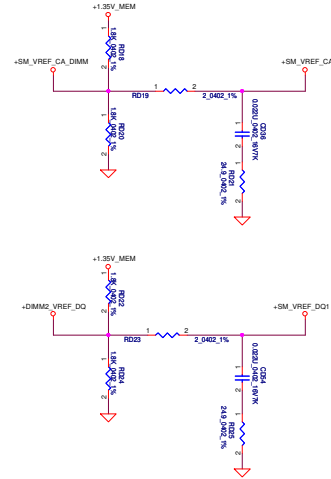
Layout Note:  
Place near JDIMM2.203,204



Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



20130730 SP07000L700 CIS Link OK



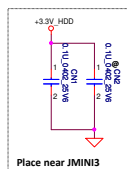
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**HDD CONN**

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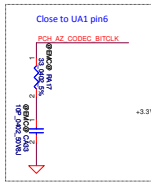
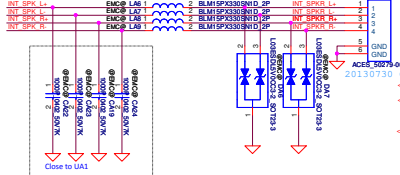




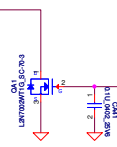
1W x 1ch, Active (Transducer spec is 80mV/0.5Vrms per unit, there are two transducer units in one speaker box.)

## Internal Speakers Header

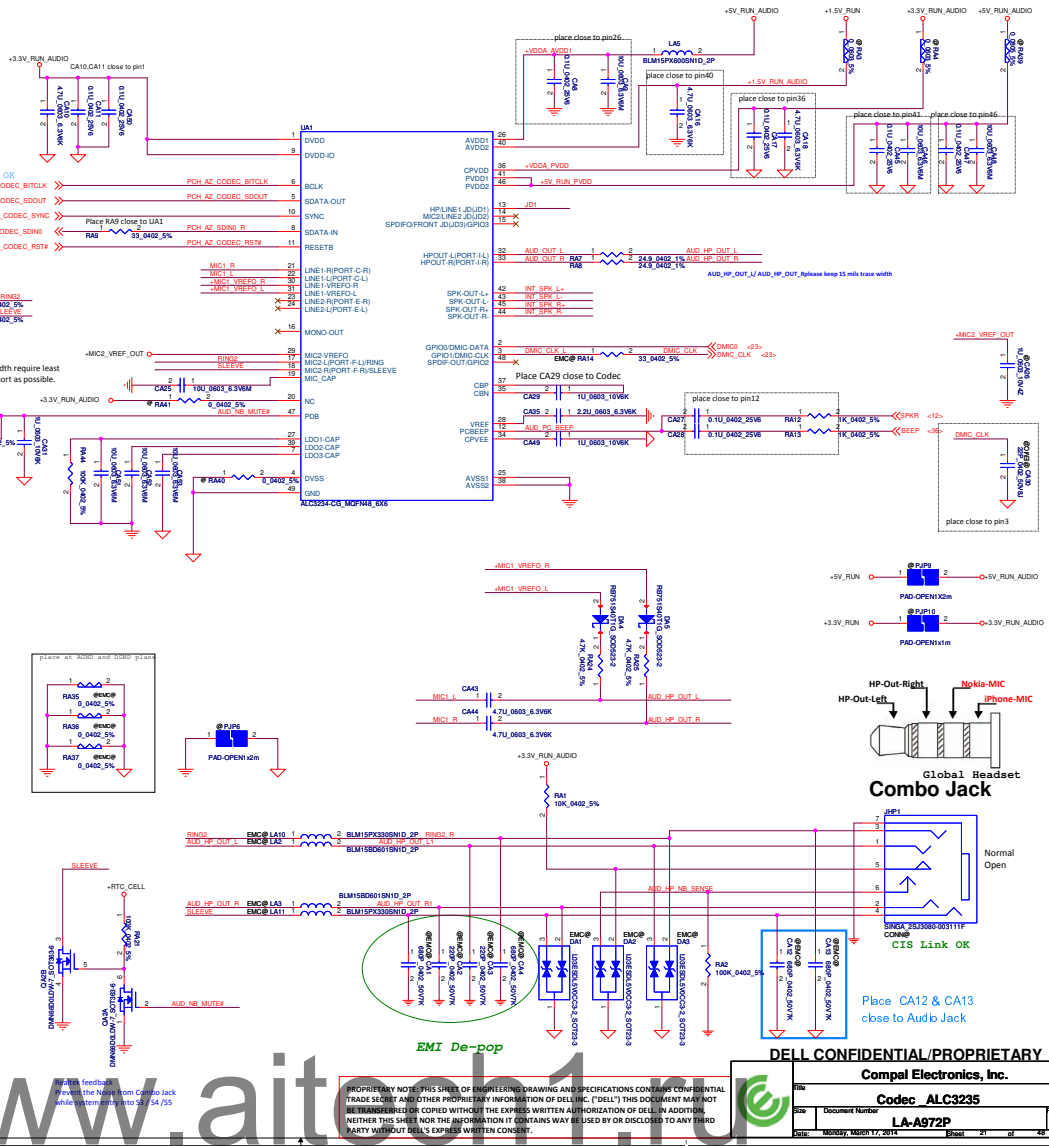
40 mils trace keep 20 mils spacing



Place closely to Pin 13.



Digital Mic (Goliad MLK no single Mic)

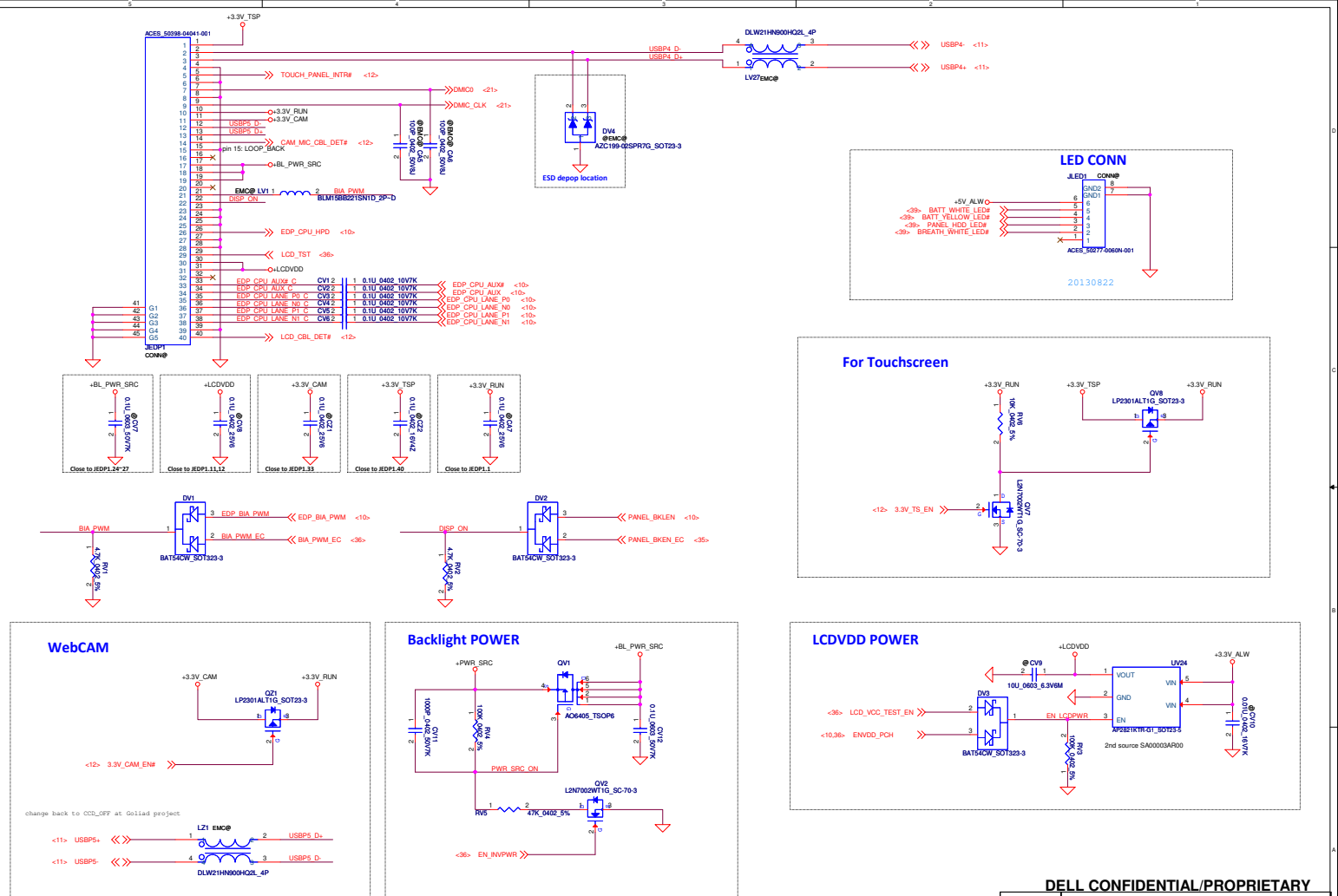


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eDP CONN & Touch screen			
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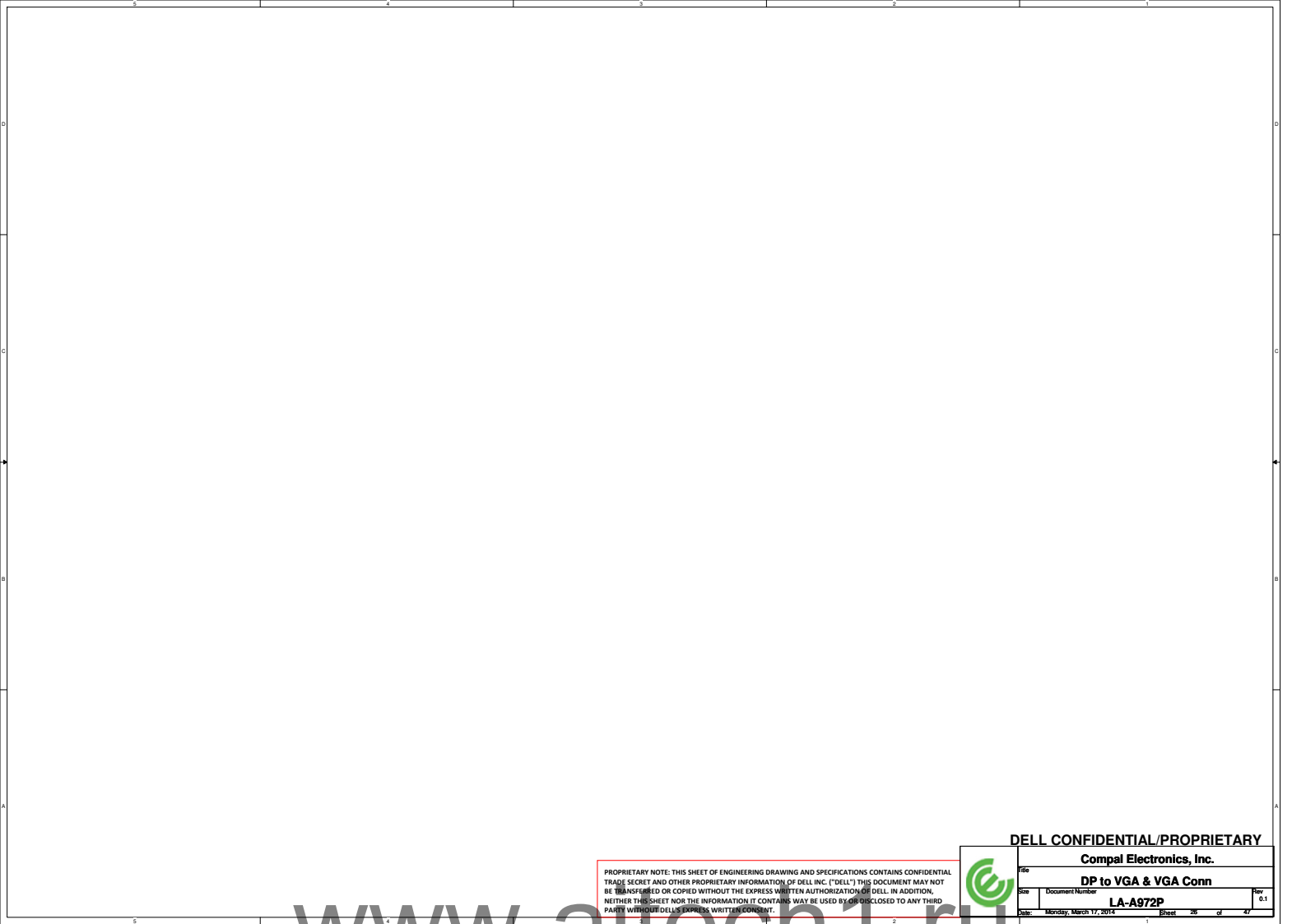
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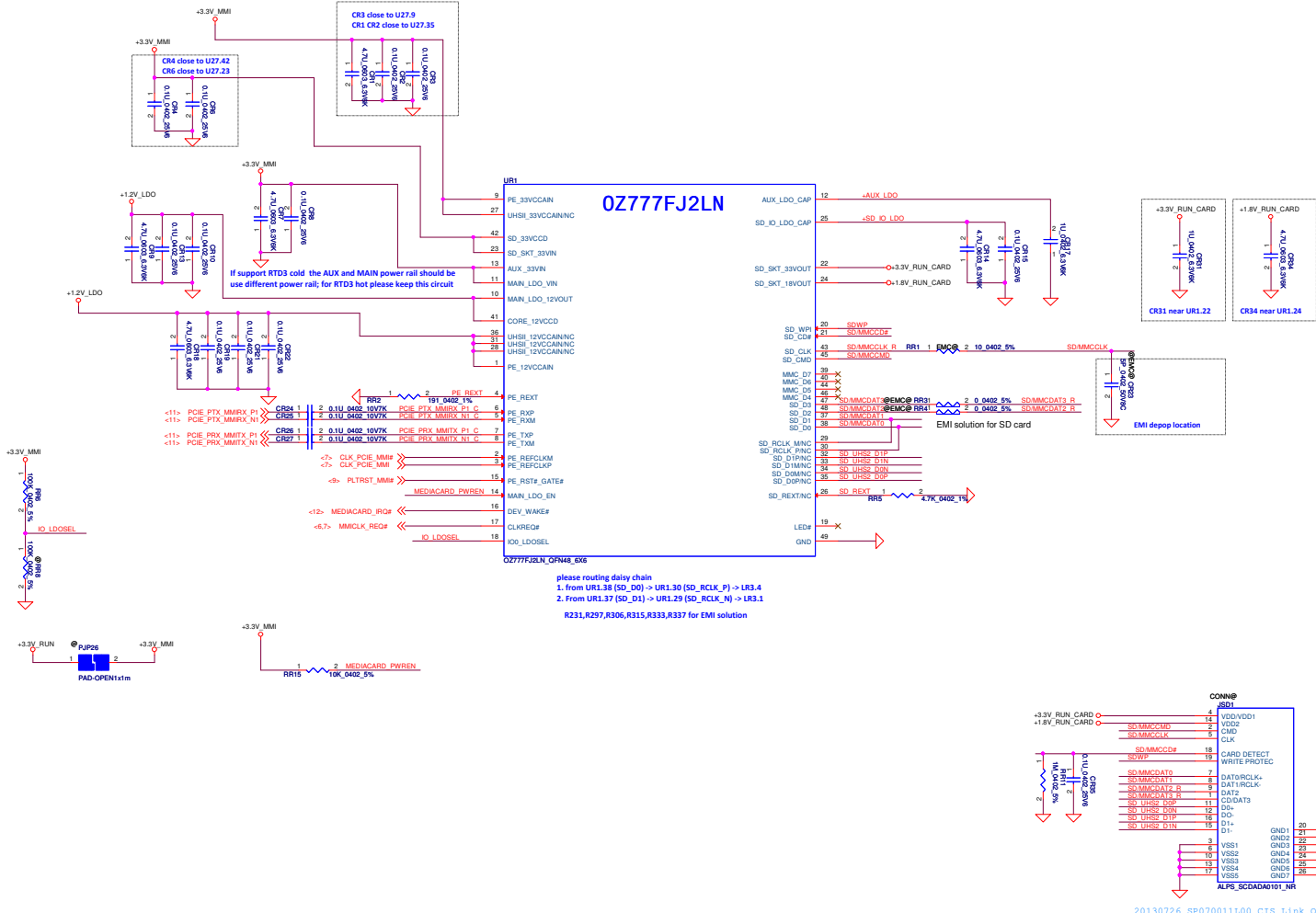
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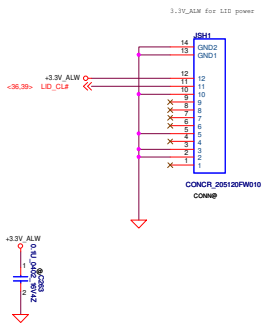
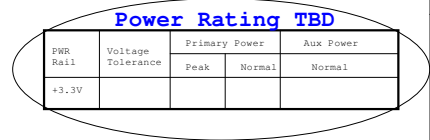




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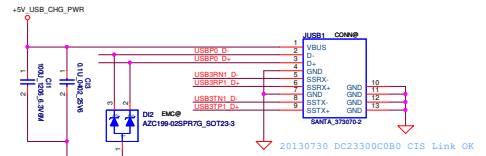
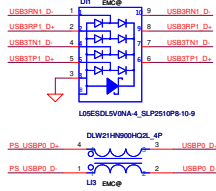
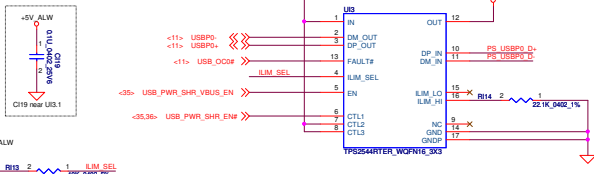
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Card Reader			
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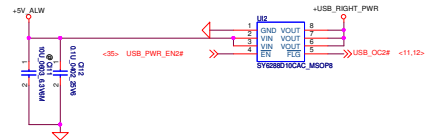
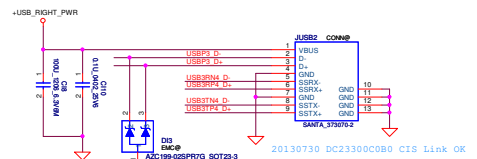
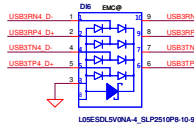
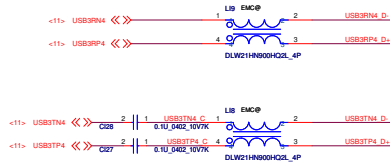


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STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE
15	HIGH	HIGH	HIGH	HIGH	NA



PCB	USB2 0	USB2 3
G12 UMA	USB3102	NX3DV221
G12 Entry	NA	NA
G14 DSC	USB3102	NX3DV221
G14 UMA	USB3102	NX3DV221
G14D_En	NA	NA
G14U_En	NA	NA

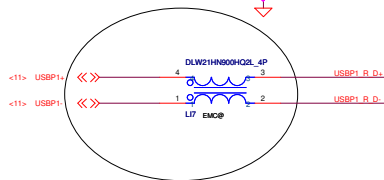
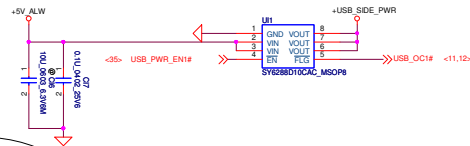
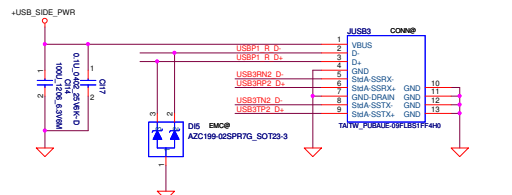
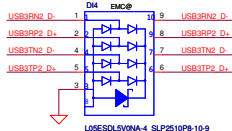
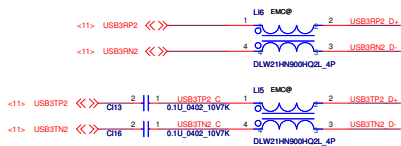


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USB3.0		Rev
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USB SW

LA-A972P

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# NFC on USH/B

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NFC		
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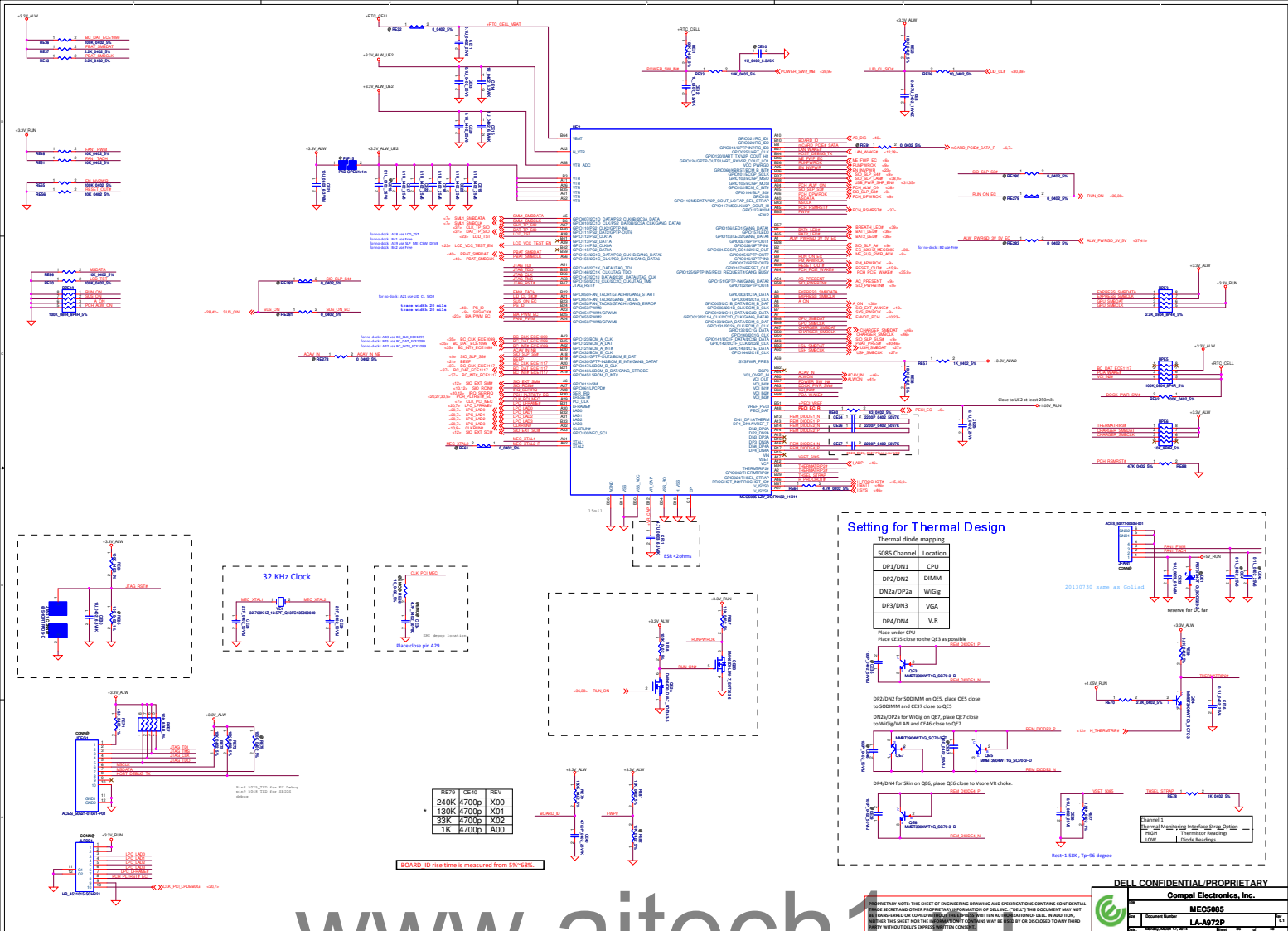


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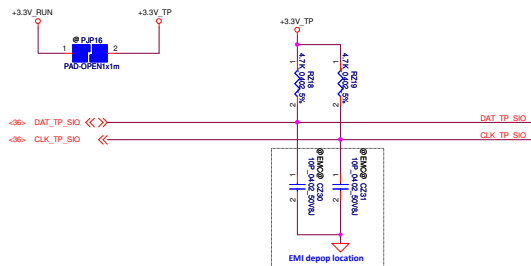
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Title: E-Dock			
Size	Document Number		Rev
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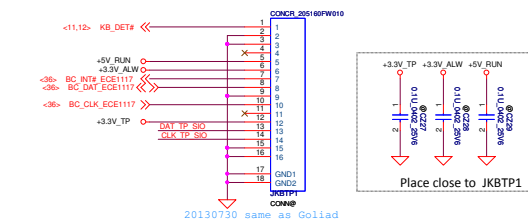




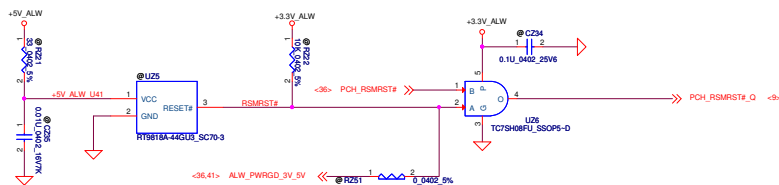
## Touch Pad



## Keyboard



## RSMRST circuit



### @HCP Cable

Part Number	Description
DC501007900	9-COMM SET 14A MB-ESP-LED-CAMERA

### @HCP TS Cable

Part Number	Description
DC501007900	9-COMM SET 14A MB-ESP-LED-CAMERA-TS

### @DC-IN Cable

Part Number	Description
DC30100M700	COMM SET 0VW DC3ACB-MB 22W1003-038110P

### @RTC BATT

Part Number	Description
DC30100M700	COMM SET 0VW DC3ACB-MB 22W1003-038110P

### @FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB74058B-MB3 A20A

### @USH Board FFC

Part Number	Description
HBK0001K000	FFC 12P G P0.5 PAD=0.3 47MM MB-USH

### @KBTP FFC

Part Number	Description
HBK0001K000	FFC 12P G P0.5 PAD=0.3 47MM MB-USB

### @NFC Board FFC

Part Number	Description
HBK0001K000	FFC 12P G P0.5 PAD=0.3 47MM MB-USB

### @BFP FFC

Part Number	Description
HBK0001K000	FFC 12P G P0.5 PAD=0.3 47MM MB-USB

### @SIM+HMB FFC

Part Number	Description
HBK0001K000	FFC 12P G P0.5 PAD=0.3 47MM MB-USB

### @Speaker

Part Number	Description
PR210003000	SPK PACK 2.5W 2.0W 4 OHM PD

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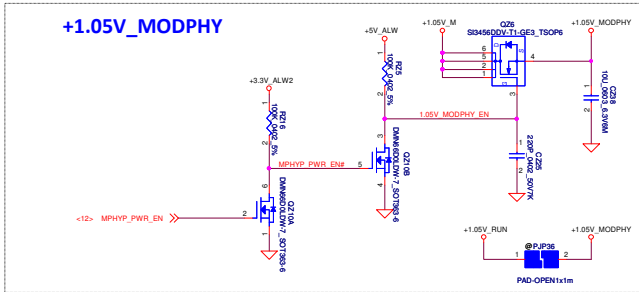
Keyboard

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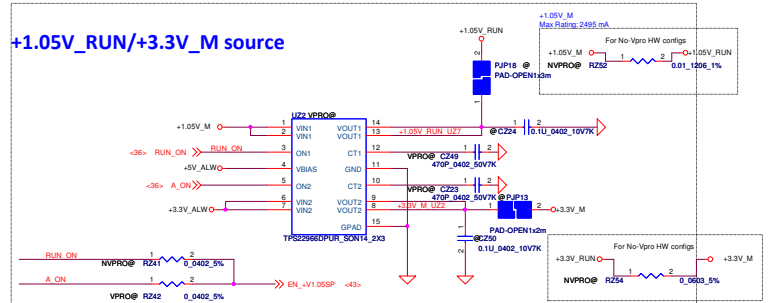
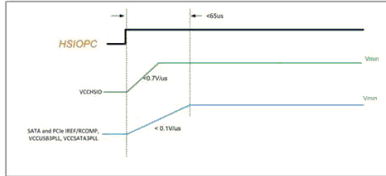
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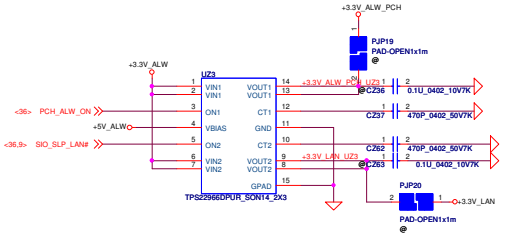


if support MODPHY off keep DSC solution  
MODPHY timing spec 0.7V/us and <65us

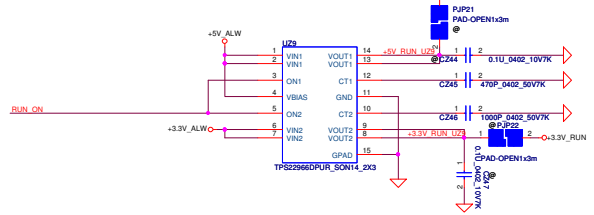
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



### +3.3V\_ALW\_PCH/+3.3V\_LAN source



### +3.3V\_RUN/+5V\_RUN source



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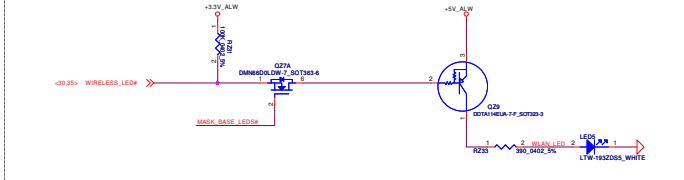


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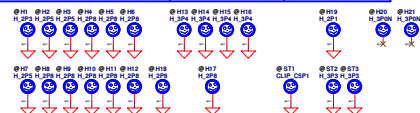
Power control			
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## WLAN LED solution for White LED



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



**Fiducial Mark**

FD1  
FIDUCIAL MARK - D

FD2  
FIDUCIAL MARK - D

FD3  
FIDUCIAL MARK - D

FD4  
FIDUCIAL MARK - D

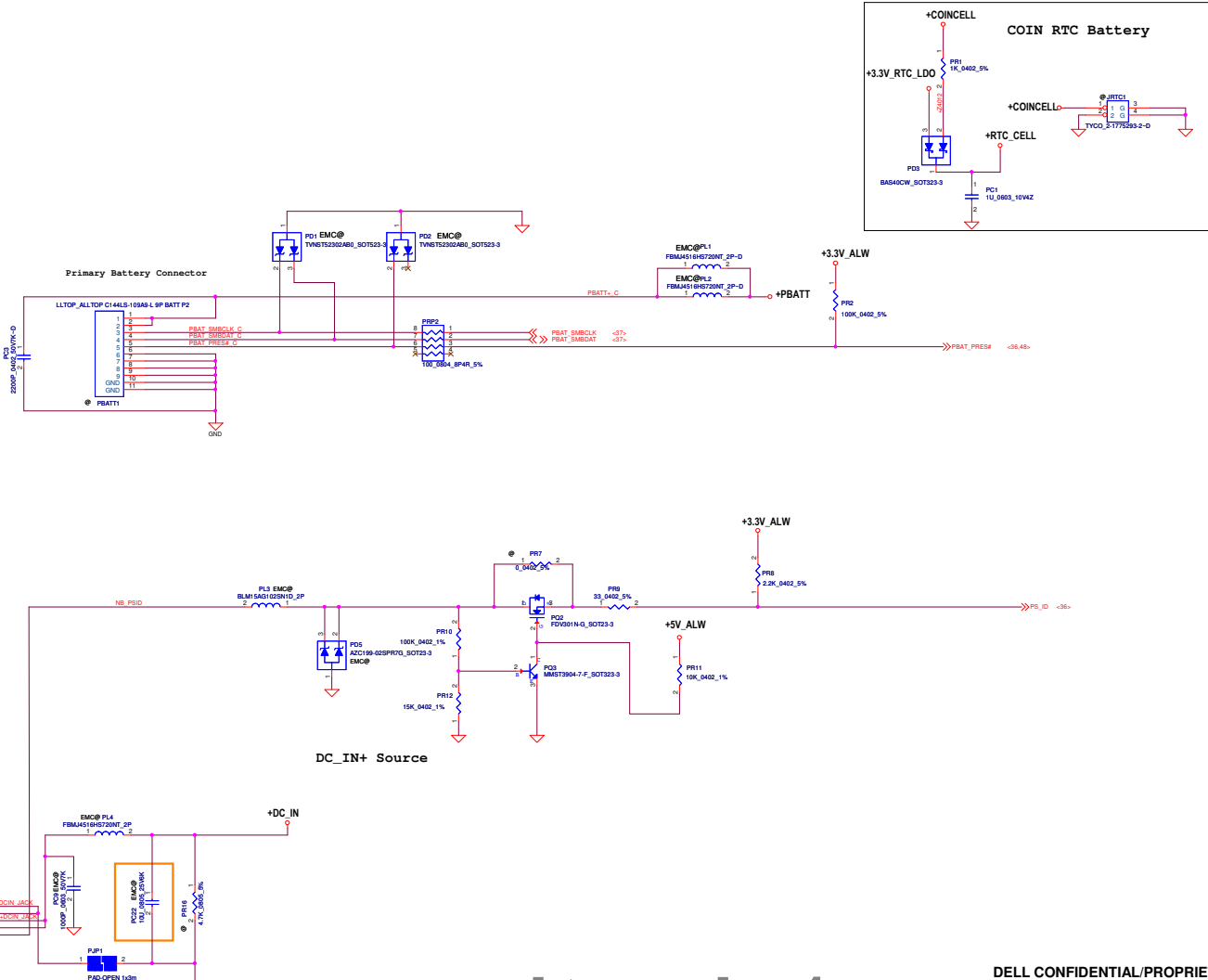
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**PAD. LED**

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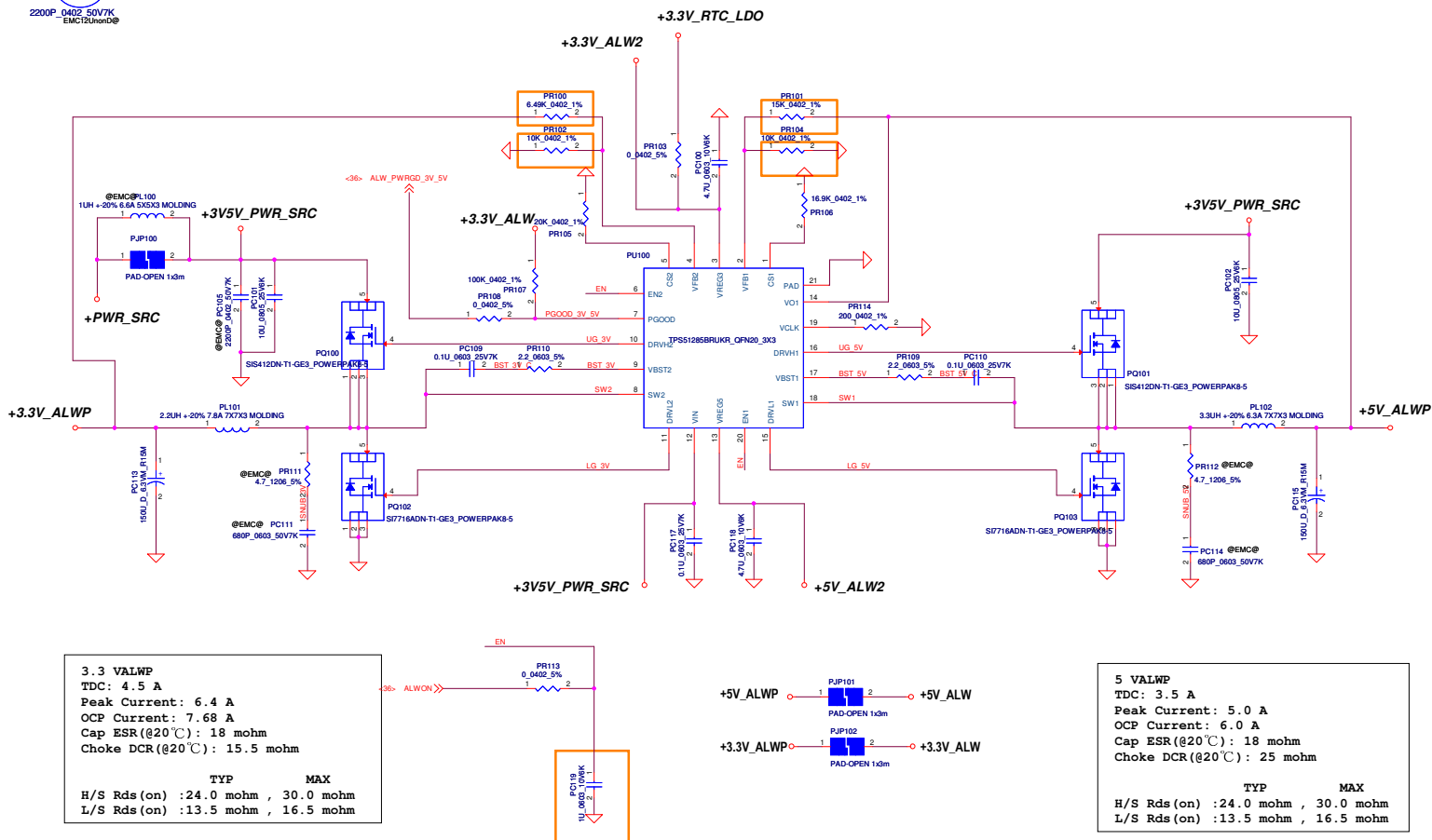
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+DCIN		
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PC105  
2200P\_0402\_50V7K  
EMC12UH06D



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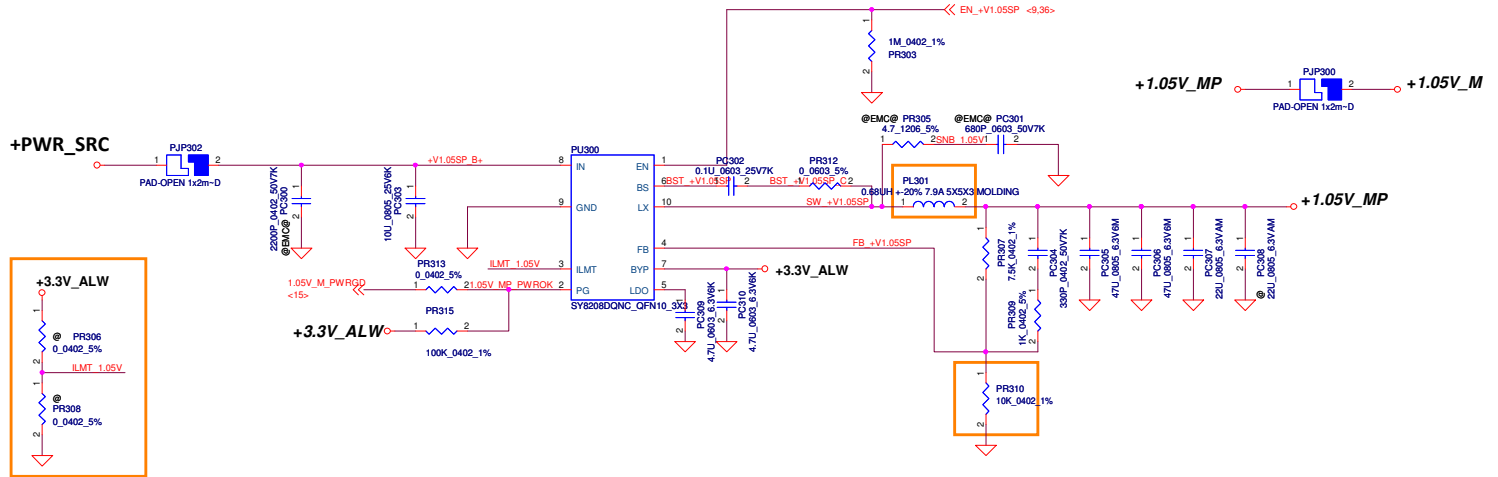
Compal Electronics, Inc.			
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+1.05V\_MEN  
TDC: 5.7 A  
Peak Current: 8.1 A  
OCP Current: 9.7 A fix by IC  
Choke DCR(@20°C): 14.0 mohm

PC300  
2200P\_0402\_50V7K  
EMC12UonD@



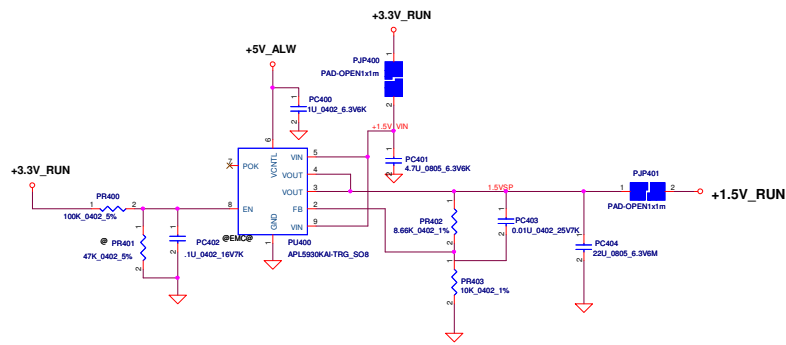
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+1.5VSP

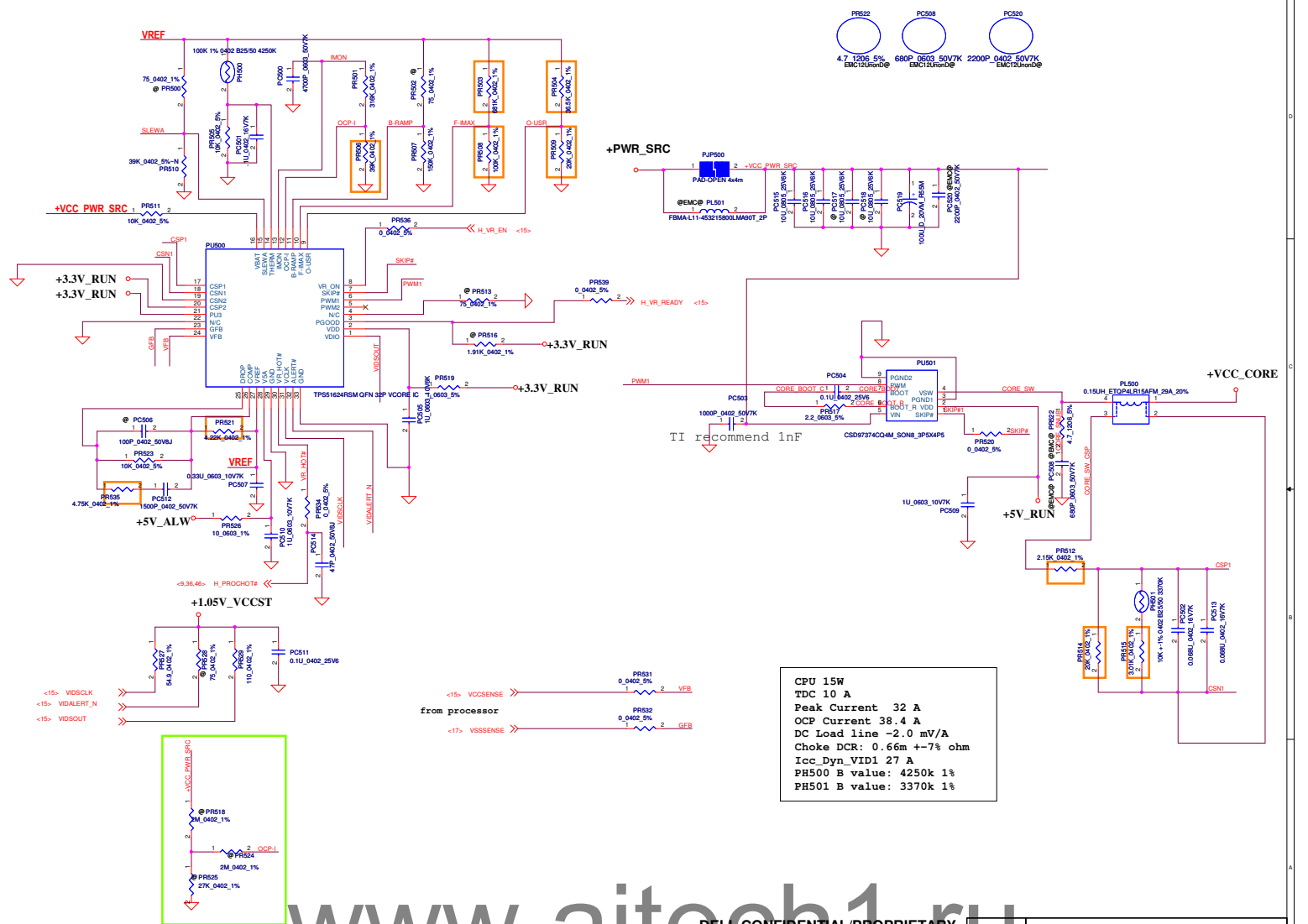
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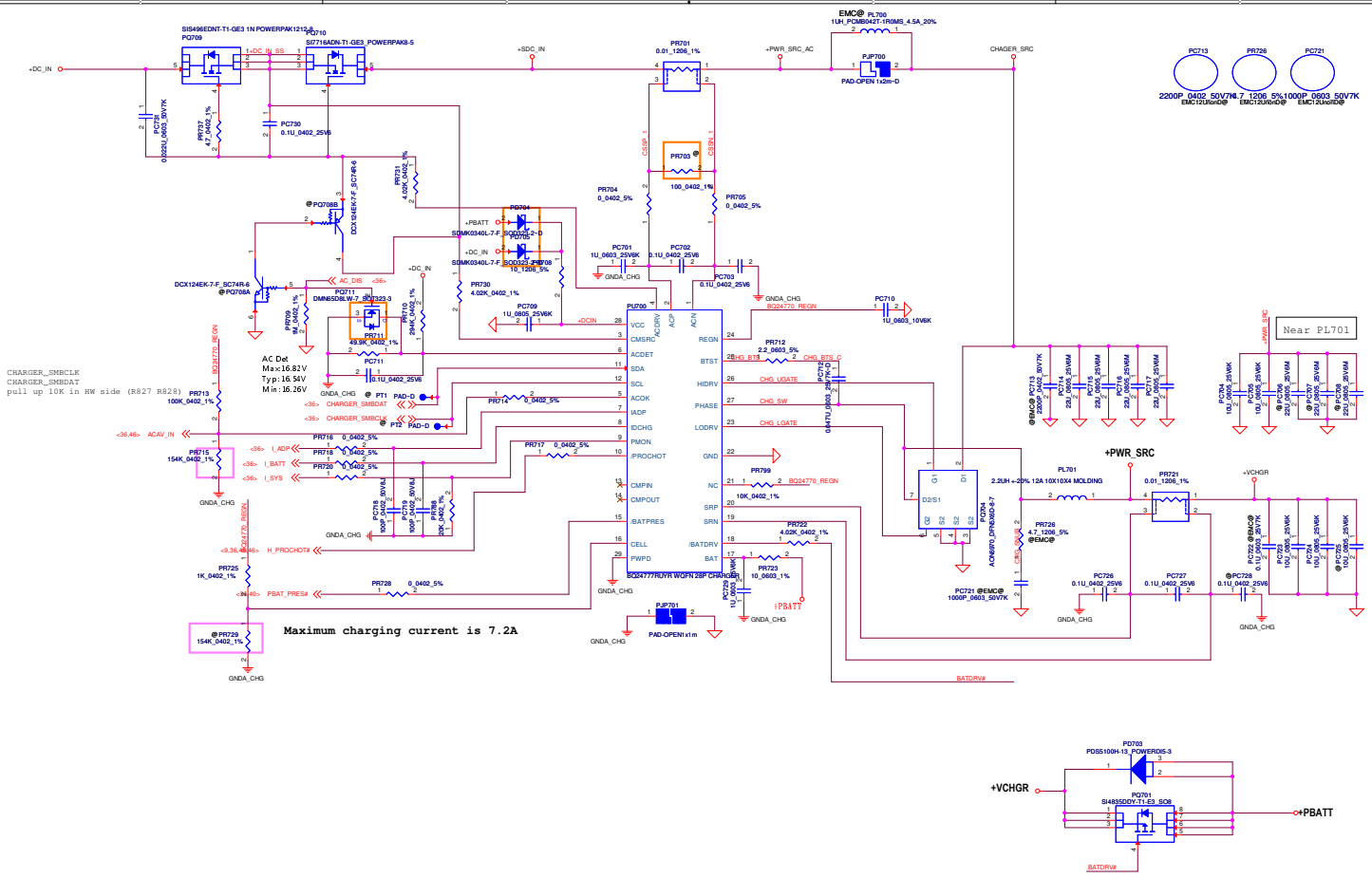


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+VCC CORE			
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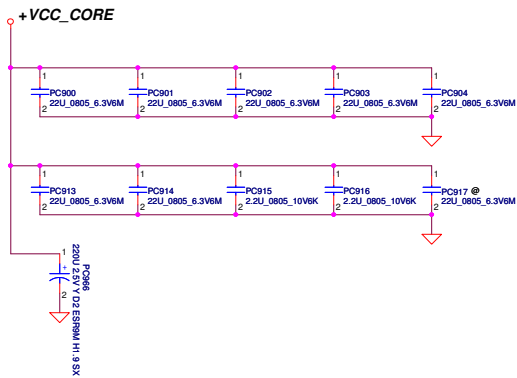


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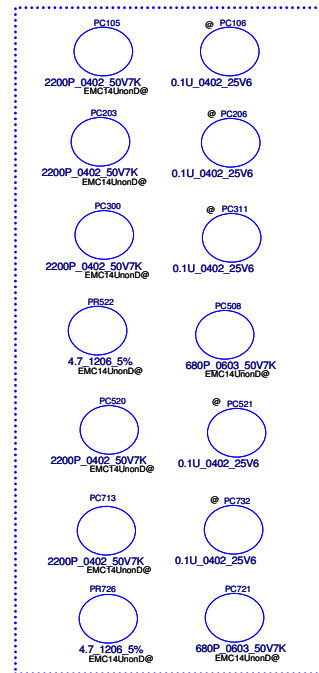
Compal Electronics, Inc.			
Charger			
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
2	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
3	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR715, PR729 to 154k	X01
4	41, 43, 44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
5	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
6	ALL	ALL	10/31	Compal	RF request	Pop PR522, PC508, PR726, PC721, PC713, PL501, PC520	X01
7	46	Charger	12/05	Compal	Has the same behavior with dock circuit	Add PQ711	X01
8	46	Charger	12/05	Compal	To add 2nd source	Remove PQ702 Add PQ709, PQ710	X01
9	46	Charger	12/05	Compal	To reduce leakage current	Remove PD701 Add PD704, PD705	X01
10	46	Charger	3/03	Compal	To set OVP level	Remove PR729	X02
11	46	Charger	3/03	Compal	To set IC function	Remove PC720 Add PR788, PR799	X02
12	40	DCIN	3/03	Compal	For ME change request	Change PBATT1	X02
13	40	DCIN	3/03	Compal	For EMC change request	Add PD5 PC20 PC21 PC22 Remove PC11	X02

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PWR P.I.R (1/1)			
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2 (X01)
2	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2 (X01)
3	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2 (X01)
4	22	HW	2013/10/9	COMPAL			0.2 (X01)
5	24	HW	2013/10/9	COMPAL	correct HDMI schematic error.	swap HDMI LANE0 & LANE2 BUS	0.2 (X01)
6	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27 From SM070003K00 (S COM FI_CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI_MURATA DLW21HN900HQ2L)	0.2 (X01)
7	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, reserved RC27.	0.2 (X01)
8	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2 (X01)
9	24	HW	2013/10/9	COMPAL	SATA circuit issue	Swap mSATA P & N	0.2 (X01)
10	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2 (X01)
11	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2 (X01)
12	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDLCO5C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2 (X01)
13	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2 (X01)
14	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	QL1 Pin2,5 & QL2 Pin2 change from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2 (X01)

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EE P.I.R (1/3)

LA-A972P

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	UZ8 Pin2 change from +3.3V_ALW to 3.3V_RUN	0.2 (X01)
16	28, 36, 38	HW	2013/10/17	COMPAL	follow Dell requirement.	Add back SUS_ON, change control pin from SUS_ON to SIO_SLP_S4# 1. UZ8.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 -- SUS_ON_EC , RPE10.2 -- SUS_ON 3. add RE282, RE281, RE280, RE279 4. UE2.B9 -- RUN_ON_EC	0.2 (X01)
17	12	HW	2013/10/24	COMPAL			0.2 (X01)
18	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2 (X01)
19	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2 (X01)
20	6, 7, 22, 28	HW	2013/10/23	COMPAL	follow xtal vender suggest	1 CC1 & CC2 change from 18PF to 3PF 2 CC8 & CC11 change from 18PF to 15PF 3 CL13 & CL14 change from 33PF to 27PF 4 RV81 change from 0 ohm to 2.2K & CV113 change to 18PF	0.2 (X01)
21	23	HW	2013/10/29	COMPAL	it's designed for E5 Goliad, E6 GMLK doesn't need.	remove RZ1	0.2 (X01)
22	30	HW	2013/10/29	COMPAL			0.2 (X01)
23	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up ( RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2 (X01)
24	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.2 (X01)
25	7	HW	2013/11/2	COMPAL	SMBUS Pull High	Add RN3&RN4 pull high to +3.3V_RUN for DDR_XDP_WAN_SMBDAT/SMBCLK	0.2 (X01)
26	21	HW	2013/11/2	COMPAL	EMC request.	Add RA42, RA43.	0.2 (X01)
27	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2 (X01)
28	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2 (X01)
39	21	HW	2013/12/17	COMPAL			0.3 (X01)
40	22	HW	2013/12/17	COMPAL			0.3 (X01)

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